**Lesson 16 – Finite State Machines (FSM) - Analysis**

**State Machine:**

**Analysis**

**Design**

1. Description
2. State Transition Diagram
3. State Transition Table & Output Table
4. Next State and Output State Equations
5. Schematic

**Slide Questions:**

**1) True it is a Moore Machine How would a Mealy look Different?**

**2) Moore Machine**

**3)**

**4)**

**5) True Look at State Machine Design/Analysis Table**

**6) 3 Flip-Flops (i.e. 23 = 8)**

**7) 8 states (5 Normal States and 3 Ghost States)**

**8) a) No - No register**

**b) No – One cyclic path doesn’t have a register**

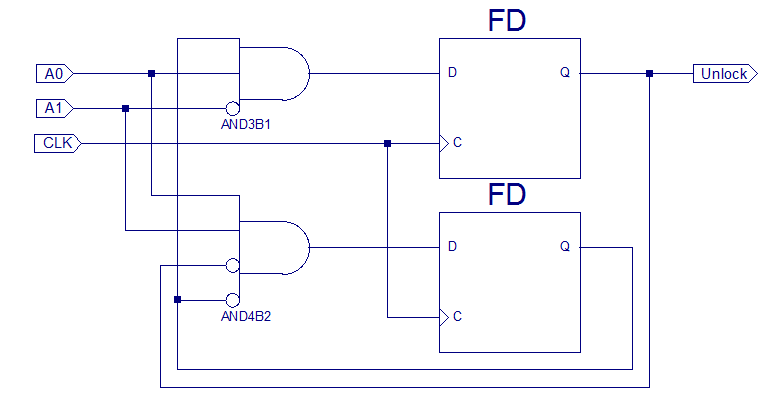
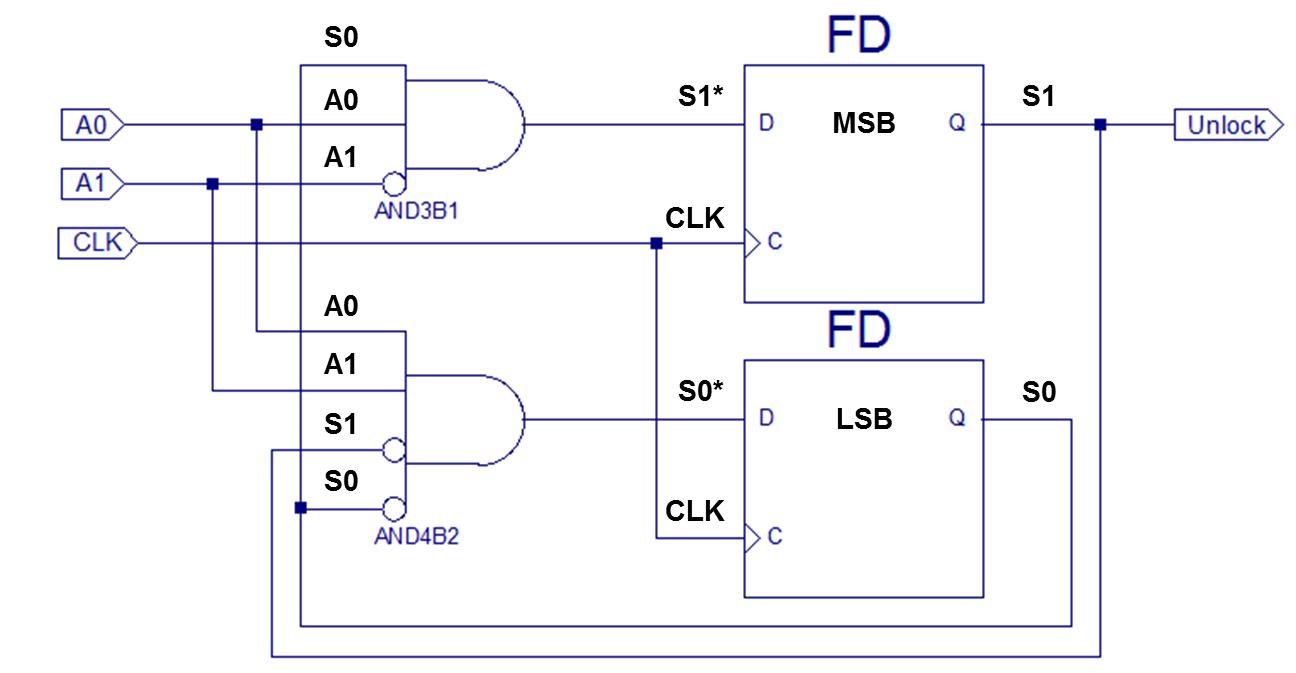
**c) Yes -**

**9) C – K-maps**

**10) B – Determine the next-state and output functions implemented by the circuit**

**Finite State Machine (FSM) Analysis – Joe Homeowner’s Garage door Opener:**

**Step 4) Schematic**

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Next State Table: | | | | | | |
| Current State | | Inputs | | Next  State | | Next State Name |
| S1 | S0 | A1 | A0 | S1\* | S0\* |
| 0 | 0 | 0 | 0 | 0 | 0 | M0 |
| 0 | 0 | 0 | 1 | 0 | 0 | M0 |
| 0 | 0 | 1 | 0 | 0 | 0 | M0 |
| 0 | 0 | 1 | 1 | 0 | 1 | M1 |
| 0 | 1 | 0 | 0 | 0 | 0 | M0 |
| 0 | 1 | 0 | 1 | 1 | 0 | M2 |
| 0 | 1 | 1 | 0 | 0 | 0 | M0 |
| 0 | 1 | 1 | 1 | 0 | 0 | M0 |
| 1 | 0 | 0 | 0 | 0 | 0 | M0 |
| 1 | 0 | 0 | 1 | 0 | 0 | M0 |
| 1 | 0 | 1 | 0 | 0 | 0 | M0 |
| 1 | 0 | 1 | 1 | 0 | 0 | M0 |
| 1 | 1 | 0 | 0 | 0 | 0 | N/A |
| 1 | 1 | 0 | 1 | 1 | 0 | N/A |
| 1 | 1 | 1 | 0 | 0 | 0 | N/A |
| 1 | 1 | 1 | 1 | 0 | 0 | N/A |

**Step 3) Next State and Output State Equations**

**Next State Equations**

**Output Equation:**

M0

**Step 2) State Transition Table & Output Table**

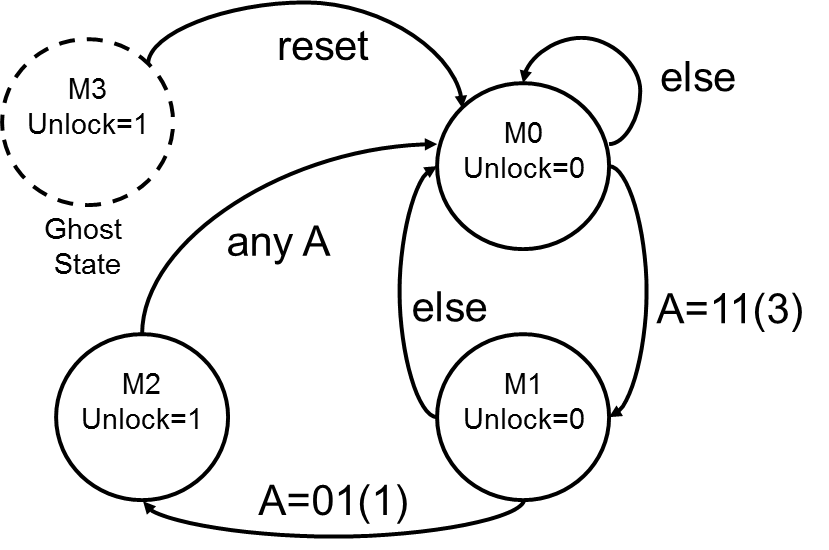
|  |  |  |  |
| --- | --- | --- | --- |
| Output Table | | | |
| Current State | | Output | State Name |
| S1 | S0 | Unlock |  |
| 0 | 0 | 0 | M0 |
| 0 | 1 | 0 | M1 |
| 1 | 0 | 1 | M2 |
| 1 | 1 | 1 | M3 |

M1

M2

M3 Ghost State – never gets here

**Step 1) State Transition Diagram**

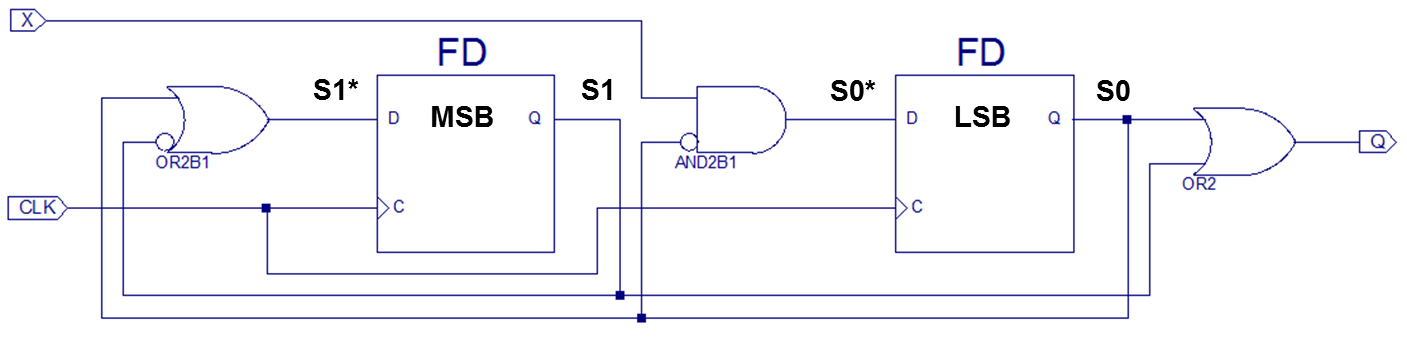
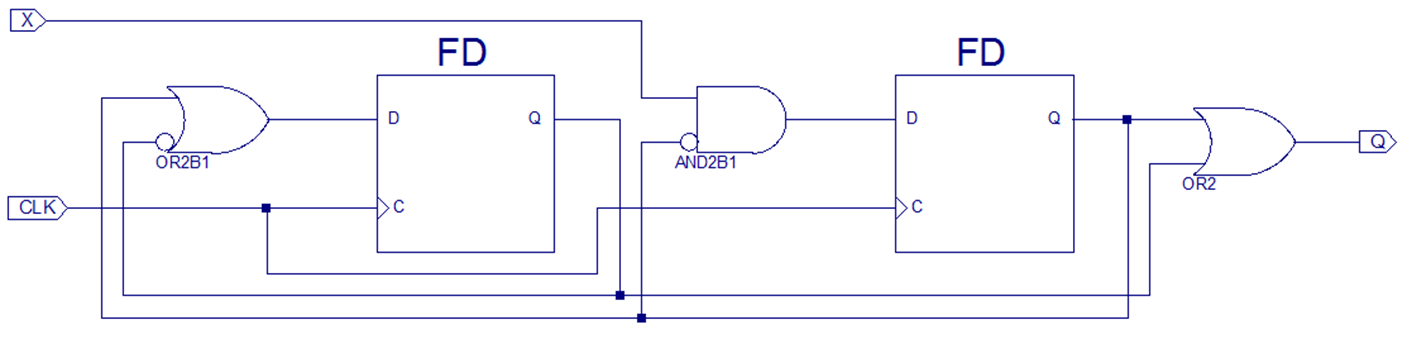
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**Step 0) Description**

**31**

**What is the Door combination?**

**Step 4) Schematic**

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Next State Table: | | | | | |
| Current State | | Inputs | Next  State | | Next State |
| S1 | S0 | X | S1\* | S0\* | Name |
| 0 | 0 | 0 | 1 | 0 | M2 |
| 0 | 0 | 1 | 1 | 1 | M3 |
| 0 | 1 | 0 | 1 | 0 | M2 |
| 0 | 1 | 1 | 1 | 0 | M2 |
| 1 | 0 | 0 | 0 | 0 | M0 |
| 1 | 0 | 1 | 0 | 1 | M1 |
| 1 | 1 | 0 | 1 | 0 | M2 |
| 1 | 1 | 1 | 1 | 0 | M2 |

**Step 3) Next State and Output State Equations**

**Next State Equations**

**Output Equation:**

M0

**Step 2) State Transition Table & Output Table**

M1

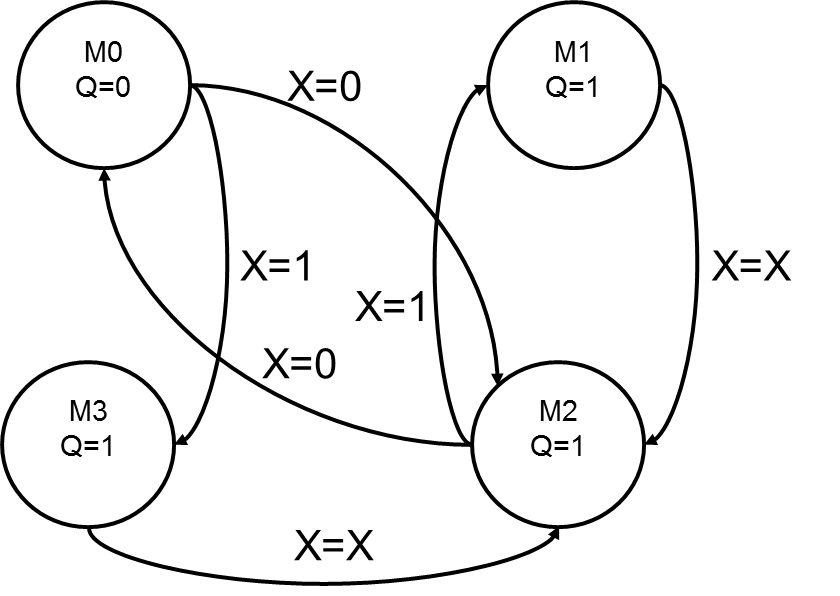
|  |  |  |  |
| --- | --- | --- | --- |
| Output Table | | | |
| Current State | | Output | State Name |
| S1 | S0 | Q |  |
| 0 | 0 | 0 | M0 |
| 0 | 1 | 1 | M1 |
| 1 | 0 | 1 | M2 |
| 1 | 1 | 1 | M3 |

M2

M3

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**Step 1) State Transition Diagram**

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**Step 0) Description**

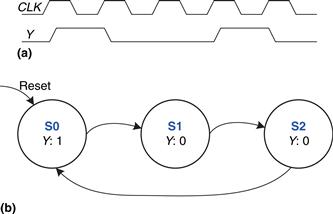
**This finite state machine is a divide-by-two counter (see Section 3.4.2)** **when X = 0. When X = 1, the output, Q, is HIGH.**

**when X = 0. When X = 1, the output, Q, is HIGH.**

**Example 3.6:**

**Divide-by-N counter** has one output and no inputs. The output Y is HIGH for one clock cycle out of every N. In other words, the output divides the frequency of the clock by N.

The waveform and state transition diagram for a divide-by-3 counter is shown in [Figure 3.28](http://techbus.safaribooksonline.com/9780123944245/ST0105_CHP003_html#F0145_CHP003). Sketch circuit designs for such a counter using binary and one-hot state encodings.



|  |  |
| --- | --- |
| **Next State Table** | |
| Current State | Next State |
| S0 | S1 |
| S1 | S2 |
| S2 | S0 |

|  |  |
| --- | --- |
| **Output Table** | |
| Current State | Output |
| S0 | 1 |
| S1 | 0 |
| S2 | 0 |